Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system comprising:

a logic design module operable ~~operational~~ to be used by one or more users to generate a logic design as part of an electrical circuit ~~in logic design tasks~~; and

a central database integrated with the logic design module and including modifiable signal parameters that are accessible for ~~to~~ use by the users of the logic design module ~~in the logic design tasks~~;

wherein the logic design module is operable to automatically update the logic design when the signal parameters in the central database are modified.

2. (Canceled).

3. (Currently Amended) The system of claim 1 ~~2~~ wherein the logic design module is structured and arranged to indicate design discrepancies automatically in the logic design resulting from the modifications to the signal parameters in the central database.

4. (Original) The system of claim 3 wherein the indicated design discrepancies include a bit width error.

5. (Original) The system of claim 1 wherein the signal parameters include a signal bit width and a value for the signal bit width.

6. (Original) The system of claim 1 wherein the signal parameters include a signal bit position and a value for the signal bit position.

7. (Currently Amended) A method comprising:

defining a signal parameter with a value;

maintaining the defined signal parameter in a central database; ~~and~~

using the defined signal parameter that is maintained in the central database in computer code for a logic design forming part of an electrical circuit;

updating the value of the defined signal parameter in the central database; and

automatically updating the logic design with the updated value of the defined signal parameter when the value of the defined signals is updated in the central database.

8. (Canceled).

9. (Currently Amended) The method of claim ~~7~~ 8 further comprising automatically indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter.

10. (Original) The method of claim 9 wherein automatically indicating design discrepancies occurring in the logic design includes graphically indicating a bit width error.

11. (Original) The method of claim 7 wherein the signal parameter includes a signal bit width and the value includes a value for the signal bit width.

12. (Original) The method of claim 7 wherein the signal parameter includes a signal bit position and the value includes a value for the signal bit position.

13. (Original) The method of claim 7 wherein the signal parameter includes a bit field and the value includes a value for the bit field.

14. (Original) The method of claim 7 further comprising accessing the central database by one or more users.

15. (Currently Amended) An apparatus comprising:

a central database accessible by one or more users;

one or more signal parameters defined in the central database;

a value for the signal parameters; ~~and~~

an interface between the central databases and a logic design module that uses the signal parameters in a logic design forming part of an electrical circuit;

wherein the value for the defined signal parameters in the central database is operable to be modified; and

wherein the logic design is automatically updated with the modified value of the defined signal parameters when the value for the defined signal parameters in the central database is modified.

16. (Original) The apparatus of claim 15 wherein the signal parameters include a signal bit width and the value includes a value for the signal bit width.

17. (Original) The apparatus of claim 15 wherein the signal parameters include a signal bit position and the value includes a value for the signal bit position.

18. (Currently Amended) A machine-accessible medium containing instructions which cause a machine to perform~~, which when accessed results in a machine performing~~ operations comprising:

defining a signal parameter with a value;

maintaining the defined signal parameter in a central database; ~~and~~

using the defined signal parameter that is maintained in the central database in computer code for a logic design forming part of an electrical circuit;

updating the value of the defined signal parameter in the central database; and

automatically updating the logic design with the updated value of the defined signal parameter when the value of the defined signal parameter is updated in the central database.

19. (Canceled).

20. (Currently Amended) The machine-accessible medium of claim 1~~8~~9 further including instructions which cause a machine

to perform operations comprising automatically indicating design discrepancies occurring in the logic design that result from updating the value of the defined signal parameter.

21. (Original) The machine-accessible medium of claim 20 wherein automatically indicating design discrepancies occurring in the logic design includes graphically indicating a bit width error.

22. (Original) The machine-accessible medium of claim 18 wherein the signal parameter includes a signal bit width and the value includes a value for the signal bit width.

23. (Original) The machine-accessible medium of claim 18 wherein the signal parameter includes a signal bit position and the value includes a value for the signal bit position.

24. (Original) The machine-accessible medium of claim 18 wherein the signal parameter includes a bit field and the value includes a value for the bit field.

25. (Currently Amended) The machine-accessible medium of claim 18 further including instructions which cause a machine to

perform operations comprising permitting one or more users to access the central database.